REMARKS

Claims 1-21 are pending and stand rejected on the same prior art grounds as made in the previous office action, namely as either anticipated by Campbell or obvious in view of a suggested combination of Campbell and Chilimbi. Applicants traverse these rejections for the same reasons previously stated. Applicants have further amended the claims in the application to further address these rejections.

Claim 1 has been amended to include the subject matter of dependent claim 6, which stands rejected based a purported combination of Campbell and Chilimbi. The office action takes the position that Campbell teaches memory management through the use of a cache eviction, under which an entry is evicted to a specific cache in response to a counter (104) measuring the number of cache misses.

As the applicants previously noted, the Campbell system manages the cache and the level of cache hierarchy in which data is placed. The present application, in contrast, identifies problem memory heap areas and optimizes them for continued storage of data. In the example of garbage collection, that optimization involves re-arranging memory regions to remove delinquent regions and improve memory performance. For example, the present application describes techniques for changing how and/or where memory regions are arranged relative to one another within the same memory heap in which those regions exist. The cache discussed in Campbell merely holds (possible coherent) copies of data in the main (or heap) memory, for faster access. Campbell does not seek to fix problems with delinquent memory at the main memory level. Instead, Campbell uses rule-based cache assignment in lieu of optimization, diverting data from a problem cache level to another cache.[1]

Further, it is noted that the affected cache levels of Campbell (102, 103 106, and 107) are totally separate from the underlying main memory (108), further reinforcing that memory heap optimization does not occur. Further still, it is reiterated that Campbell does not correct memory problems. "Improving efficiency" does not necessarily mean correcting or removing delinquent memory regions. Placing a cache in a better state does not address the underlying problems of the memory heap affecting that cache. The Campbell solution

maybe thought of as a superficial one – a gloss designed to mask underlying defects – while the present application goes to the root of the problematic memory regions in the heap and corrects them.

To clarify the recited subject matter, claim 1 has been amended as follows.

> 1. (Currently amended) An article comprising a machine-accessible medium having stored thereon instructions that, when executed by a machine, cause the machine to:
>
> obtain, from a performance monitor, performance data for a memory heap having a plurality of memory regions;
>
> based on the performance data, determine if at least one of the plurality memory regions is a delinquent region; and
>
> in response to a determination that at least one of the plurality of memory regions is a delinquent region, execute a memory management routine to optimize that region of the memory heap by executing a garbage collection routine on at least one delinquent region, the garbage collection routine re-arranging the plurality of memory regions stored in the memory heap to optimize the memory heap.

Clearly, Campbell cannot be said to teach the recited subject matter, or any re-arranging of memory regions.

Regarding the purported combination with Chilimbi, the office action simply offers no teaching, suggestion, or motivation to combine the two references. And, either way, there is nothing suggesting that the combination would teach the actual subject matter recited above. The entirety of the office action's position on the rationale for combination is at section 5a of the action, where the office action points to the paragraph spanning pages 1 and 2 of Chilimbi. That paragraph generally describes Chilimbi's cache-conscious garbage collection approach. There is **no** suggestion whatsoever of modifying Chilimbi's garbage collection processes with the automated cache eviction logic and counter processes of Campbell, as would have to occur to sustain the office action's rejection. At most, the recitation from Chilimbi would point the reader to adding garbage collection as a totally different feature to the Campbell system. There would be no reason to integrate the cache

[1] Further discussions regarding Campbell are provided in applicants' July 17, 2006 amendment.

eviction routines with the collection techniques of Chilimbi, so that garbage collection would be automatically initiated through the three purported Campbell features identified by the examiner: automatically monitoring performance data, determining if there are delinquent regions, and in response executing a memory management routine. Absent the office action identifying any source for modifying Chilimbi and Campbell, in the suggested way, then it would appear that the office action has only relied solely upon hindsight for this suggested combination. Yet, one cannot point to different references teaching different features and simply conclude that a combination of the references would necessarily interrelate these features in the particular way claimed in an application.

The rejection of claim 1 is traversed on procedural and substantive grounds.

Applicants also highlight the rejection of dependent claim 8. Dependent claim 8 recites establishing a size granularity of the memory region prior to obtaining the performance data for the memory region. This allows the present system to adjust fineness of the memory regions to be re-arranged. The office action points to Campbell 3:47-54, however, this section merely states that "eviction is performed on the basis of the amount of empty space, or conversely, the allocated space." There is nothing that suggests establishing a size granularity of a memory region, or doing so prior to obtaining performance data. The examiner is requested to clarify where it is believed that the recited subject mater is taught or remove the rejection completely. The rejection as it stands appears to be improper for failure to make a *prima facie* showing.

Claim 14 has been amended as follows, and is believed to be in condition for allowance for similar reasons to that stated above with respect to claim 1:

> 14. (Currently amended) A method comprising:
>
> within a central processor for a machine, identifying load miss memory addresses from a memory heap including a plurality of memory regions;
>
> maintaining a frequency count for the identified load miss memory addresses;
>
> determining if any of the plurality of memory regions include a threshold value of load miss memory addresses; and

optimizing the memory heap in response to a determination that at least one of the plurality of memory regions includes a threshold value of load miss memory addresses, wherein optimizing the memory heap comprises performing a garbage collection on at least one of the memory regions including the threshold value of load miss memory addresses.

Claim 19 has been amended as recounted below, and is believed to be in condition for allowance. In particular, even assuming arguendo that there were a motivation to combine the two references (and applicants believe there is no such motivation) there is nothing teaching or suggesting using the cache eviction logic and counter hardware of Campbell to initial garbage collection or otherwise re-arrange memory regions upon a finding of a delinquent memory region. Since Campbell does not use its hardware for correcting memory problems, but rather for adjusting cache hierarchy to optimize performance in light of these problems, it cannot be said that Campbell's monitoring features would have been combined with the garbage collection routines of Chilimbi, without resort to improper hindsight. There is nothing in the art which suggests or motivates modifying the teachings of Chilimbi and Campbell in these ways.

19. (Currently amended) A system comprising:

hardware to monitor performance of a memory heap and to compile performance data on memory regions within the memory heap, wherein the hardware is able to determine if any of the memory regions are delinquent regions based on the compiled performance data and wherein the hardware has a memory manager for optimizing the delinquent regions by re-arranging memory regions in the memory heap in response to a determination of at least one delinquent member region; and

a memory manager for optimizing the delinquent regions.

For the foregoing reasons, the rejections of the pending claims are traversed. Claims 1-5, 7-15, and 17-21 are in condition for allowance. Reconsideration of the independent claims is requested. Reconsideration of the dependent claims is requested.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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